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EXAMINER	
NGUYEN, MIKE	
ART UNIT	**PAPER NUMBER**
2182	15

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,787	MOUNT, JOHN A.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Applicant's amendment 10/08/2003 in response to Examiner's Office Action has been reviewed. The following rejections now apply.

2. Claims 1-20 are pending for the examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes et al. (U.S. Pat. No. 5,828,856) in view of Gittinger et al. (U.S. Pat. No. 5,668,815).

As to claim 1, Bowes teaches in a storage system having a bus (see fig. 2A element 214) operatively coupled to a first controller chip and a first channel chip (see fig. 2A element 220 and fig. 2B element 244 wherein the channel chip 244 is built in the controller chip 220), the channel chip having several registers (see fig. 3 elements 324, 314, 322, 312, 316, 326, 366), the storage system also having a storage medium operatively coupled to the bus through a storage medium interface (see fig. 2A elements "Hard Disk Drive", 214, 228), a method for retrieving data record on a storage medium comprising the step of:

(a) retrieving a first portion of the record data via the bus (see fig. 3 col. 5 lines 42-65);

(c) retrieving a second portion of the record data via the bus (see col. 5 lines 42-65); and

Although the method taught by Bowes shows substantial features of the claimed invention (discussed above), it fails to explicitly teach (b) updating some of the registers via the bus. Gittinger; however, teaches (b) updating some of the registers via the bus (see fig. 3 col. 11 lines 20-25). Given the teaching of Gittinger, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the method, such as taught by Gittinger, in order to provide reducing the burden on the primary processor.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes and Gittinger, and further in view of Cloke (U.S. Pat. No. 6,411,452).

5. As to claim 2, the combination of Bowes and Gittinger fails to explicitly teach a read head, further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c). Cloke; however, teaches the interface includes a read head, further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c) (see col. 27 line 55 to col. 28 line 2)). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination by employing the well-known or conventional feature of the interface, such as taught by Cloke, in order to provide improving the method of storing and retrieving data.

6. As to claim 3, the combination of Bowes and Gittinger fails to explicitly teach a plurality of operating parameters that are modified in updating step (b). Cloke; however, teaches the interface has plurality of operating parameters that are modified in updating step (b) (see fig. 5 elements 252-258). Given the teaching of Cloke, a person having ordinary skill in the art would

have readily recognized the desirability and advantages of modifying the combination by employing the well-known or conventional feature of the interface, such as taught by Cloke, in order to provide eliminating of additional or dedicated serial ports, improving start-up or initialization times, and reducing fabrication costs due to the elimination of unneeded circuitry for the storage system.

7. As to claims 4 and 5, the combination of Bowes and Gittinger fails to explicitly teach at least one read channel parameter value selected from the group consisting of: a precompensation value; a filter coefficient value; and a phase offset value, and at least one mode-indicative value. Cloke; however, teaches the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value; and at least one mode-indicative value (see col. 25 lines 2-12). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination by employing the well-known or conventional feature of the registers, such as taught by Cloke, in order to provide eliminating of additional or dedicated serial ports, improving start-up or initialization times, and reducing fabrication costs due to the elimination of unneeded circuitry for the storage system.

Claims 6, 8-9 and 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes in view of Cloke.

8. As to claim 6, Bowes teaches in a storage system having an interface configured to read data, a direct memory access (DMA) controller, and a microprocessor coupled to the DMA controller (see fig. 2A elements 228, 218, 222), a method comprising steps of:

(a) retrieving via the DMA controller several values (see fig. 3 col. 5 lines 42-65);

(c) reconfiguring the interface to read data (see col. 5 lines 42-65);

(d) reading the target segment (see col. 5 lines 42-65); and

Bowes fails to explicitly teach a disc with at least two zones having zone identifiers Z_A and Z_B, a value table indexed by zone identifiers, and (b) updating at least some the read channel register values from the retrieved values. Cloke; however, teaches teach a disc with at least two zones having zone identifiers Z_A and Z_B (see figs 2, 3), a value table indexed by zone identifiers, and (b) updating at least some the read channel register values from the retrieved values (see fig. 5 col. 27 line 55 to col. 28 line 2). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the method, such as taught by Cloke, in order to provide maintaining disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disk surface.

9. As to claim 8, Bowes fails to explicitly teach at least one head, in which positioning step (c) includes a step of (c1) moving the at least one head radically across the disc, the moving step (c1) beginning before retrieving step (a) is complete. Cloke; however, teaches the interface includes at least one head, in which positioning step (c) includes a step of (c1) moving the at least one head radically across the disc, the moving step (c1) beginning before retrieving step (a) is complete (see co. 27 line 55 to col. 28 line 2). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the interface, such as taught by Cloke, in order to provide improved the method of storing and retrieving data.

10. As to claim 9, Bowes fails to explicitly teach moving step (c1) begins before retrieving step (a) begins. Cloke; however, teaches the moving step (c1) begins before retrieving step (a) begins (see col. 27 line 55 to col. 28 line 2). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the interface, such as taught by Cloke, in order to provide improved the method of storing and retrieving data.

11. As to claim 11, Bowes teaches the method of claim 6 further comprising prior steps of: (e) configuring the interface to read data; and (f) receiving a signal from the interface (see col. 5 lines 42-65). Although the method taught by Bowes shows substantial features, it fails to explicitly teach (g) deriving several values indicative of the interface's performance in zone Z_B from the received signal; and (h) storing some of the derived values in the value table each at a position associated with zone Z_B. Cloke; however, teaches teach (g) deriving several values indicative of the interface's performance in zone Z_B from the received signal; and (h) storing some of the derived values in the value table each at a position associated with zone Z_B (see col. 27 line 55 to col. 28 line 2). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the method, such as taught by Cloke, in order to provide improved the method of storing and retrieving data.

12. As to claim 12, Bowes teaches the method of claim 6 in which the storage system includes an integrated circuit comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the DMA controller (see figure 2A elements 222 column 5 lines1-21).

13. As to claim 13, Bowes fails to explicitly teach (j) sensing position data from servo sector via the interface; and (k) deriving a servo control signal from the sensed position data with the microprocessor during step (b). Cloke; however, teaches (j) sensing position data from servo sector via the interface; and (k) deriving a servo control signal from the sensed position data with the microprocessor during step (b) (see fig. 1D col. 9 lines 8-58). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the method, such as taught by Cloke, in order to provide improved the method of storing and retrieving data.

14. As to claim 14, Bowes teaches the storage system of claim 6 configured to perform the method further comprising a printer circuit board assembly including a memory containing the value table, the storage system (see figure 2A) comprising: a master integrated circuit (IC) containing the microprocessor and the direct memory access controller, the DMA controller being operatively coupled to the memory (see figure 2A elements 222, 218, 224); and a bus coupled between the master IC and the slave IC, the bus controllable by the DMA controller to perform updating step (b) (see figure 3 elements 312, 322, 314, 324 and figure 2A element 214). Although the storage system taught by Bowes shows substantial features (disclosed above), it fails to explicitly teach a slave IC containing the several read channel registers. Cloke; however, teach a slave IC containing the several read channel registers (see fig. 5 elements 252-258 col. 25 lines 2-12). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-

known or conventional feature of the method, such as taught by Cloke, in order to provide improved the method of storing and retrieving data.

15. As to claim 15, Bowes teaches a disc drive comprising:

a disc stack comprising at least one disc (see figure 2A element "Hard Disk Drive");

an interface configured to read data from the at least one disc (see figure 2A element 214);

a memory (see fig. 2A elements 224, 226)

a first controller chip containing a microprocessor and direct memory access (DMA) controller, the DMA controller operatively coupled to memory (see figure 2A elements 220, 218, 224 and figure 2B element 257);

a first channel chip having several registers (see figure 2B element 244 and figure 3 elements 324, 314, 322, 312); and

a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory (see figure 2B element 214).

Although the disc drive taught by Bowes shows substantial features of the claimed invention (discussed above), it fails to explicitly teach several values indexed by the zone identifier, and to update several of the registers in response to a zone transition event. Cloke; however, teaches several values indexed by the zone identifier (see col. 25 lines 2-12), and to update several of the registers in response to a zone transition event (see col. 27 line 55 to col. 28 line 2). Given the teaching of Cloke, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or

conventional feature of the disc drive, such as taught by Cloke, in order to provide reducing the burden on the primary processor.

16. Claim 16 is directed to a method implementing the storage system as set forth in claim 1. Since Bowes and Cloke teach the storage system as set forth in claim 1; therefore, they also teach the method as set forth in claim 16.

17. As to claims 17-18, Bowes teaches the bus is serial and parallel (see fig. 2A element 214).

18. As to claim 19, Bowes teaches the method of claim 16 wherein the steps are controlled by a processor (see fig. 2A element 222).

19. As to claim 20, Bowes teaches the method of claim 16 wherein the steps are controlled by a direct memory access apparatus (see fig. 2A element 218).

20. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes and Cloke, and further in view of Asakawa et al. (U.S. Pat. No. 5,121,260)

As to claim 7, the combination of Bowes and Cloke fails to explicitly teach a predetermined starting track number, further comprising a step of deriving zone identifier Z_B from the predetermined starting track number before retrieving step (a). Asakawa; however, teaches the target segment has a predetermined starting track number, further comprising a step of deriving zone identifier Z_B from the predetermined starting track number before retrieving step (a) (see fig. 1 col. 3 lines 54-63 wherein a zone identifier is defined to correlate with a selected track which is positioned by the disc drive read/write head). Given the teaching of Asakawa, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination by employing the well-known or conventional

feature of the method, such as taught by Asakawa, in order to provide maintaining disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disk surface.

21. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes and Cloke, and further in view of Machado et al. (U.S. Pat. No. 5,255,136).

As to claim 10, the combination of Bowes and Cloke fails to explicitly teach a corresponding Rb that is not in common with zone Za, in which positiong step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate Rb. Machado; however, teaches zone Zb has a corresponding Rb that is not in common with zone Za, in which position step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate Rb (see fig. 1 col. 10 line 54 to col. 11 line 23). Given the teaching of Machado, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination by employing the well-known or conventional feature of the method, such as taught by Machado, in order to provide increasing data storage capacity and optimizing data transfer rate.

Response to Arguments

22. Applicant's arguments with respect to claims 1-6 and 13-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,643,081 B1 (Walker et al.)

U.S. Pat. No. 5,870,628 (Chen et al.)

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 703 305-5040. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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03/11/2004